UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,952,742 B2
APPLICATION NO. : 10/787116
DATED : October 4, 2005
INVENTOR(S) : Tadahiko Hisano

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page delete the old fig. 19 and insert the new figure that is illustrated on the title page that is attached.

Claim 11 (in column 28 at line 49 to 51) should appear as follows:

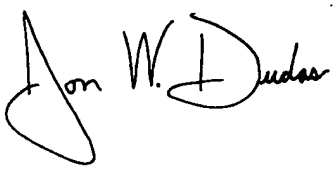
11. The storage device according to claim 10, further comprising, a switch connected to the port for setting the status.

Claim 27 (column 30 at line 8 to 16) should appear as follows:

27. The apparatus according to claim 26, wherein the storage device inputs a command from the data input, provides the data to the memory in accordance with the command to store the data in the memory or to output data in the memory to the data output, and the apparatus provides the control signal to the control input from the interface, and the command and the data to the data input from the interface, to store the data in the memory or to output data in the memory to the data output.

Signed and Sealed this

Tenth Day of June, 2008



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(12) **United States Patent**
Hisano

(10) **Patent No.: US 6,952,742 B2**
(45) **Date of Patent: Oct. 4, 2005**

(54) **EXTERNAL STORAGE DEVICE AND METHOD OF ACCESSING SAME**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/787,116**

(22) Filed: **Feb. 27, 2004**

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Related U.S. Application Data

(62) Division of application No. 10/197,479, filed on Jul. 18, 2002, now Pat. No. 6,735,638, which is a division of application No. 09/644,650, filed on Aug. 24, 2000, now Pat. No. 6,557,047, which is a division of application No. 08/913,170, filed as application No. PCT/JP96/00519 on Mar. 5, 1996, now Pat. No. 6,138,173.

(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**[7] **G06F 13/14**

(52) **U.S. Cl.** **710/3**; 710/13; 710/20; 710/33; 710/74; 710/300

(58) **Field of Search** 710/2, 3, 13, 20, 710/33, 74, 300

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Primary Examiner—Rehana Perveen

(57) **ABSTRACT**

A storage device (**200**) has a memory and a circuit (**100**) which has a data input (Din), a control input (CTRL) and a data output (Dout), and provides an address input from the data input (Din) to the memory in accordance with a control signal from the control input (CTRL), so that the storage device (**200**) stores the data at the address in the memory or outputs data at the address in the memory to the data output (Dout). The apparatus provides the control signal to the control input (CTRL) from the interface (PORTS, P0, P1, P2), address and the data to the data input (Din) from the interface (PORTS, P0, P1, P2), to store the data at the address in the memory or to output data at the address in the memory to the data output (Dout). The apparatus may have a microcontroller (MPU) in which the interface (PORTS, P0, P1, P2) is provided.

39 Claims, 25 Drawing Sheets